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10/627,269	07/25/2003	Hong-Yi Hubert Chen	MP0357	7592

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EXAMINER	
PATEL, HETUL B	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/627,269	CHEN ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-17,19-53,55,57-62 and 64-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-17,19-53,55,57-62 and 64-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/13/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the claim amendment and remarks filed on November 13, 2006. This amendment has been entered and carefully considered. Claims 5, 18, 54, 56 and 63 are cancelled; claims 1, 6, 14, 19, 27, 38, 49, 55, 57, 64, 65 and 69 are amended; and claim 75 is newly added. Therefore, claims 1-4, 6-17, 19-53, 55, 57-62 and 64-75 are currently pending in this application.

2. Applicant's arguments filed on November 13, 2006 have been fully considered but they are not persuasive.

3. The rejection of claims 1-4, 6-17, 19-53, 55, 57-62 and 64-74 as in the previous office action is respectfully maintained but updated to show the changes made by the amendment and reiterated below for Applicant's convenience.

Information Disclosure Statement

4. The information disclosure statements (IDS) submitted on 03/31/2006 and 09/13/2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-4, 6-17, 19-48 and 75 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 recites "A register file for a data processing system comprising: a unbanked memory unit ..., input ports ..., output ports ..., and an address encoder...." It is unclear how a register file, which is a data/software file, can have hardware components such as unbanked memory unit, input/output ports and address encoder. Claims 2-4, 6-13 and 75 are also rejected as they further limit the rejected base claim 1. Claim 14 also includes similar limitations as claim 1 and rejected for the same reasons as claim 1. Claims 15-17 and 19-26 are also rejected as they further limit the rejected base claim 14. Similarly, the independent claims 27 and 38 includes "the register file (means) including: an unbanked memory unit ..., input ports ..., and output ports ....". It is unclear how a register file (means), which is a data/software file, can have hardware components such as unbanked memory unit, input ports and output ports. Claims 28-37 and 39-48 are also rejected as they further limit the rejected base claims 27 and 38.

Claim Objections

6. Claim 1 is objected to because of the following informalities:

The phrase "an address encoder, for each input port" should be written as "an address encoder for each of said input ports" in the last paragraph of claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-4, 8-17, 21-26, 49-53, 55, 57-62 and 64-74 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaggar (USPN: 5,701,493).

As per claim 1, Jaggar teaches a register file for a data processing system comprising an unbanked memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode); input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs for addressing at least one register using an encoded address; and output ports (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from at least one register addressable by an encoded address (e.g. see the abstract and Figs. 1 and 8). Jaggar further teaches an address encoder (i.e. the combination of components 12-20 in Fig. 8) for each input port, the address encoder to provide an encoded address (i.e.

the combination of register address and the mode bits, 17 in Fig. 8) for accessing one of the plurality of registers (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8). Examiner interpreting the limitation "an address encoder for each input port" as the *same* address encoder for each input port.

As per claim 2, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) identifies a general purpose register (i.e. registers R0-R13 in Figs. 1 and 8) associated with a processor mode (i.e. a user mode and system mode) (e.g. see the abstract and Figs. 1 and 8).

As per claim 3, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each register (i.e. R0-R15 in Fig. 8) is associated with a register index (i.e. 0000-1111, 17 in Fig. 8) that maps to an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) based on at leasf one processor mode (i.e. a user mode and system mode) (e.g. see Figs. 1 and 8).

As per claim 4, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the input ports (i.e. the "reg add", mode bits input to 17 and input to 8 in Fig. 8) receive at least one source register index input (i.e. the register address input) and processor mode input (i.e. the mode bits input) for use in providing an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing at least one register (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8).

As per claim 8, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that data for one or more instructions being processed is outputted from the unbanked memory unit (i.e. the MMU 62 in Fig. 8) (e.g. see Fig. 8).

As per claim 9, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the register file further comprising input ports (i.e. the "reg add", mode bits input to 17 and input to 8 in Fig. 8) to receive at least one write index input (i.e. the register address input) and processor mode input (i.e. the mode bits input) for use in providing the encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for writing data to at least one register (i.e. to R0-R15 in Fig. 8); and at least one write input port (i.e. input port to the read buffer 8 shown in Fig. 8) for writing the data to the register (i.e. R0-R15 in Fig. 8) addressable by the encoded address (e.g. see Fig. 8).

As per claim 10, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that data for one or more executed instructions (i.e. instructions/commands buffered in instruction register 12 in Fig. 8) for the data processing are written into the unbanked memory unit (i.e. MMU 62 in Fig. 8) (e.g. see Fig. 8).

As per claim 11, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the processor mode includes exception handling modes (i.e. a plurality of IRQ32 etc.) (e.g. see the abstract).

As per claim 12, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the exception handling processor modes include the

interrupt request (IRQ) mode (i.e. IRQ32), the fast interrupt request (FRQ) mode (i.e. FRQ32), the undefined instruction (UND) mode (i.e. Undef32) and the abort exception (ABT) mode (i.e. Abt32) (e.g. see the abstract and Col. 2, lines 45-58).

As per claims 14-17 and 21-25, see arguments with respect to the rejection of claims 1-4 and 8-12, respectively. Claims 14-17 and 21-25 are also rejected based on the same rationale as the rejection of claims 1-4 and 8-12, respectively.

As per claims 13 and 26, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each exception handling mode corresponds to one or more registers (e.g. see Col. 2, lines 45-58).

As per claim 49, Jaggar teaches a microprocessor comprising an integrated circuit comprising a unbanked memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode); and at least one address encoder (i.e. the combination of components 12-20 in Fig. 8) to provide at least one encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for addressing at least one of the plurality of registers (i.e. R0-R15 in Fig. 8); a plurality of inputs (i.e. the reg address from 14 and the mode bits from 18 as shown in Fig. 8) to receive index (i.e. reg address 17 shown in Fig. 8) and processor mode information (i.e. the mode bits 17 shown in Fig. 8) for use in providing the encoded address (i.e. the combination of

register address and the mode bits, 17 in Figs. 1 and 8), at least one output to output data stored in the storage location addressable by the encoded address (e.g. see the abstract and Figs. 1 and 8). Jaggar further teaches an address encoder (i.e. the combination of components 12-20 in Fig. 8) for each input port, the address encoder to provide an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing one of the plurality of registers (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8). Examiner interpreting the limitation "an address encoder for each input port" as the *same* address encoder for each input port.

As per claims 50-53 and 55, see arguments with respect to the rejection of claims 2-3, 11-12 and 9, respectively. Claims 50-53 and 55 are also rejected based on the same rationale as the rejection of claims 2-3, 11-12 and 9, respectively.

As per claim 57, see arguments with respect to the rejection of claim 49. Claim 57 is also rejected based on the same rationale as the rejection of claim 49.

As per claims 58-62 and 64, see arguments with respect to the rejection of claims 2-3, 11-12 and 9, respectively. Claims 58-62 and 64 are also rejected based on the same rationale as the rejection of claims 2-3, 11-12 and 9, respectively.

As per claim 65, Jaggar teaches an integrated circuit method comprising configuring the integrated circuit to receive processor mode (i.e. a user mode and system mode) and source data inputs (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8); configuring the integrated circuit to determine an encoded address based on the processor mode and source data inputs, wherein the encoded address corresponds to a respective one of a plurality of registers (i.e. memory

locations) and a corresponding processor mode (i.e. a user mode and system mode); configuring the integrated circuit to address one of the registers using an encoded address; and configuring the integrated circuit to output data from the register addressable by the encoded address (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) (e.g. see the abstract and Figs. 1 and 8).

As per claim 66, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches about configuring the integrated circuit to output data for multiple instructions (i.e. via the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8).

As per claim 67, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches about configuring the integrated circuit to write data to one of the registers addressable by an encoded address (e.g. see the abstract).

As per claim 68, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches about configuring the integrated circuit to write data to one of the registers for multiple executed instructions (i.e. via the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8).

As per claims 69-74, see arguments with respect to the rejection of claims 1, 65, 65 and 66-68, respectively. Claims 69-74 are also rejected based on the same rationale as the rejection of claims 1, 65, 65 and 66-68, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 6-7 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar in view of Meier et al. (USPN: 6,363,471) hereinafter, Meier.

As per claims 6 and 7, Jaggar teaches the claimed invention as described above, but failed to teach a latch circuit and a selector as clamed. Meier, however, teaches about using the latch or other clocked storage devices to store the intermediate values for pipelining to the next stage (e.g. see Col. 16, lines 21-35 and Fig. 6). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Meier's latch circuit in the register file taught by Jaggar. In doing so, this latch circuit can buffer the data (i.e. the encoded addresses) for pipeline storage in case if the data can be reused. The further limitation of having the selector coupled to the latch and the address encoder is well-known and notorious old in the art at the time of the current invention was made. By using the selector, such as a mux, the encoded address can be selected either from the latch circuit or directly from the address encoder based on a select signal. The Examiner herein taking Official Notice on this subject matter.

As per claims 19-20, see arguments with respect to the rejection of claims 6-7, respectively. Claims 19-20 are also rejected based on the same rationale as the rejection of claims 6-7, respectively.

9. Claims 27-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar in view of Kerr et al. (USPN: 2003/0159021) hereinafter, Kerr.

As per claim 27, Jaggar teaches a data processing system comprising a microprocessor (i.e. 62 in Fig. 8) comprising a register file, the register file including a unbanked memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode); input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs for addressing at least one register using an encoded address; and output ports (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from at least one register addressable by an encoded address (e.g. see the abstract and Figs. 1 and 8). Jaggar further teaches an address encoder (i.e. the combination of components 12-20 in Fig. 8) for each input port, the address encoder to provide an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing one of the plurality of registers (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8). Examiner interpreting the

limitation "an address encoder for each input port" as the *same* address encoder for each input port.

However, Jaggar does not teach that the microprocessor comprising a plurality of pipeline stages. Kerr, on the other hand, teaches the microprocessor (i.e. the TMC core, 600 in Fig. 6) comprising a plurality of pipeline stages (i.e. 610, 620, 630 and 660 in Fig. 6) (e.g. see paragraph [0003] and Fig. 6). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the plurality of pipeline stages taught by Kerr in the data processing system of Jaggar. In doing so, a number of instructions are being executed in parallel and as a result of that the overall performance of the data processing system increases.

As per claim 28, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) identifies a general purpose register (i.e. registers R0-R13 in Figs. 1 and 8) associated with a processor mode (i.e. a user mode and system mode) (e.g. see the abstract and Figs. 1 and 8).

As per claims 29, 31 and 32, the combination of Jaggar and Kerr teaches the claimed invention as described above and furthermore, Kerr teaches that the pipeline stages include an instruction fetch stage (i.e. IF 610 in Fig. 6) to fetch one or more instructions; an instruction decode stage (i.e. ID 620 in Fig. 6) to decode fetched instructions from the instruction fetch stage, the instruction decode stage to forward inputs to the memory unit (i.e. 640 in Fig. 6) for outputting data from or writing data to

one or more of the registers (i.e. 652, 654 in Fig. 6), an execution stage (i.e. EX 630 in Fig. 6) including a plurality of execution units (i.e. 646 and 656 in Fig. 6), each execution unit to receive data from the register file for executing an instruction, and a write back or retire logic stage (i.e. WB 660 in Fig. 6) to receive results data associated with one or more instructions executed by the execution units of the execution stage, and to forward the results data to the register file for storage (i.e. via bus 426 in Fig. 6) (e.g. see Fig. 6 and paragraphs [0038]-[0040]).

As per claim 30, the combination of Jaggar and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that the register file further includes a plurality of input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs from the instruction decode stage, the inputs being used to obtain the encoded address for accessing at least one register; and at least one output port (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from the register addressable by the encoded address (e.g. see Figs. 1 and 8).

As per claim 33 the combination of Jaggar and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that the register file further includes a plurality of input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive the data from the write back or retire logic for one or more executed instructions, the data to be written in the register file (e.g. see Figs. 1 and 8).

As per claim 34, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each register (i.e. R0-R15 in Fig. 8) is associated with a register index (i.e. 0000-1111, 17 in Fig. 8) that maps to an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) based on at least one processor mode (i.e. a user mode and system mode) (e.g. see Figs. 1 and 8).

As per claim 35, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the processor mode includes exception handling modes (i.e. a plurality of IRQ32 etc.) (e.g. see the abstract).

As per claim 36, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that the exception handling processor modes include the interrupt request (IRQ) mode (i.e. IRQ32), the fast interrupt request (FRQ) mode (i.e. FRQ32), the undefined instruction (UND) mode (i.e. Undef32) and the abort exception (ABT) mode (i.e. Abt32) (e.g. see the abstract and Col. 2, lines 45-58).

As per claim 37, the combination of Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each exception handling mode corresponds to one or more registers (e.g. see Col. 2, lines 45-58).

As per claims 38-48, see arguments with respect to the rejection of claims 27-37, respectively. Claims 38-48 are also rejected based on the same rationale as the rejection of claims 27-37, respectively.

Allowable Subject Matter

10. Claim 75 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Remarks

11. As to the remark, Applicant asserted that with regards to independent claims 1 and 27,

(a) Jaggar fails to show, teach or suggest **an** address encoder for each input port as recited in claim 1 and other independent claims.

Examiner respectfully traverses Applicant's remark for the following reasons:

With respect to (a), Jaggar does teach an address encoder (i.e. the combination of components 12-20 in Fig. 8) for each input port, the address encoder to provide an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing one of the plurality of registers (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8). Examiner would like to point out to Applicant that upon broadest interpretation the limitation "an address encoder for each input port", it is equated with "the *same/common* address encoder for each input port".

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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